Application No. 10/699,756   MXIC 1521-1
                                                         (P900384US)

In the claims:

      This listing of claims will replace all prior versions and listings of claims in the application:

1   1. (currently amended) An integrated circuit, comprising:

2   an input port by which data is received from a source external to the integrated circuit;

3   a configurable logic array having a programmable configuration defined by configuration

4   data stored in electrically programmable configuration points within the configurable logic array;

5   memory ~~adapted to store~~ storing instructions for a mission function for the integrated

6   circuit, ~~to store~~ and storing instructions for an initialization function used to transfer the

7   configuration data to the programmable configuration points within the configurable logic array

8   in response to an initialization event; and

9   a processor coupled to the memory which fetches and executes said instructions from the

10   memory.

1   2. (original) The integrated circuit of claim 1, including:

2   a programmable configuration memory on the integrated circuit adapted to store the

3   configuration data, wherein said initialization function transfers the configuration data from the

4   programmable configuration memory to the configurable logic array.

1   3. (original) The integrated circuit of claim 1, wherein said memory comprises a non-volatile

2   store.

1   4. (original) The integrated circuit of claim 1, wherein said memory comprises a floating gate

2   memory store.

1   5. (original) The integrated circuit of claim 1, wherein said memory comprises a read-only

2   memory store.

1   6. (original) The integrated circuit of claim 1, wherein said memory comprises a first non-

2   volatile store for the initialization function, and a second store for the mission function.

1   7. (original) The integrated circuit of claim 1, wherein said memory comprises a first volatile

2   store for the initialization function, and a second store for the mission function.

1   8. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the

2   processor, and wherein the initialization function includes using the watchdog timer to generate

3   an initialization event in response to errors, and upon the initialization event, re-executing the

4   initialization function.

1   9. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the

2   processor, and wherein the initialization function includes loading the configuration data onto the

3   integrated circuit via the input port on the integrated circuit and using the watchdog timer to

4   generate an initialization event in response to errors, and upon the initialization event, reloading

5   the configuration data via the input port.

1   10. (original) The integrated circuit of claim 1, wherein the initialization function includes

2   receiving encrypted configuration data via the input port on the integrated circuit, and decrypting

3   the configuration data.

1   11. (original) The integrated circuit of claim 1, wherein the initialization function includes

2   receiving compressed configuration data via the input port on the integrated circuit, and

3   decompressing the configuration data.

1   12. (original) The integrated circuit of claim 1, wherein the electrically programmable

2   configuration points comprise non-volatile, charge programmable memory cells.

1   13. (original) The integrated circuit of claim 1, wherein the electrically programmable

2   configuration points comprise nonvolatile, programmable memory cells.

1   14. (original) The integrated circuit of claim 1, including:

2   an interface between the processor and the configurable logic array supporting said

3   initialization function.

Application No. 10/699,756   MXIC 1521-1
                                                                   (P900384US)

1   15. (original) The integrated circuit of claim 1, wherein said memory stores instructions for an

2   in-circuit programming function to write or modify instructions for the initialization function.

1   16. (original) The integrated circuit of claim 1, wherein said memory includes a protected

2   memory array storing instructions for a backup configuration load function, and a second

3   memory array storing instructions for said initialization function, the protected memory array

4   being protected from alteration by an in-circuit programming function and the second memory

5   array being accessible to be written or modified by the in-circuit programming function.

1   17. (original) The integrated circuit of claim 1, wherein said processor comprises a configurable

2   logic array configured to execute said instructions.

///